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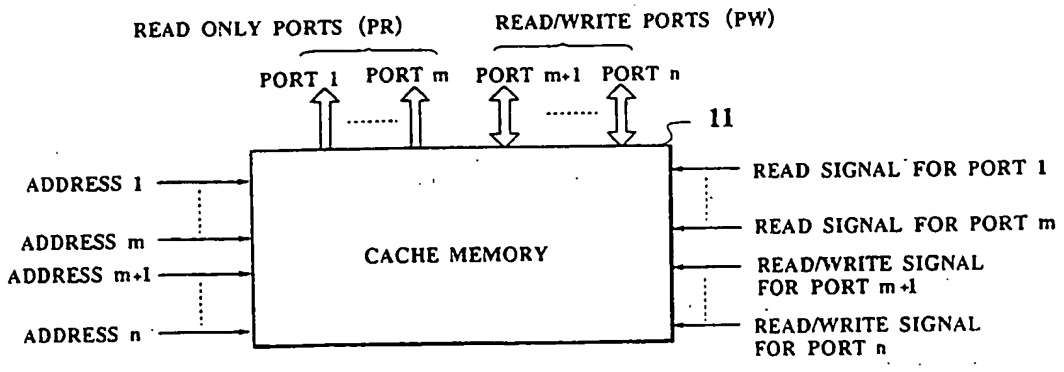
(54) Multiport cache memory.

(57) A multiport cache memory for exchanging data or instructions with a plurality of arithmetic circuitries independently according to a load instruction or a store instruction provided from a CPU comprising a plurality of read only ports (PR) for respectively transmitting the data or the instructions to each arithmetic circuitry according to the load instruction, and a plurality of read/write ports (PW) for respectively transmitting the data or the instructions from/to each arithmetic circuitry according to the load or store instruction.

FIG.4



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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a multiport cache memory in which two types of ports are provided for reducing the structure thereof.

2. Description of the Background Art

In general, as shown in Fig. 1, a conventional CPU 1 for accessing to a main memory 2 comprises:

an internal arithmetic circuitry 3; and

a cache memory 4 for exchanging data or instruction with the main memory 2 at a low access speed of the main memory 2 and exchanging the data or the instruction with the arithmetic circuitry 3 at a high speed of the arithmetic circuitry 3, the main memory 2 being provided with large scale dynamic random access memory (DRAM).

In the above configuration, the arithmetic processing speed in the arithmetic circuitry 3 is not regulated by the low speed access speed in the main memory 2 because the arithmetic circuitry 3 exchanges the data or the instruction with the cache memory 4.

However, even if clock cycle is shortened, it is difficult for processing capacity to be improved more than the shortening of the clock cycle because only one data or one instruction can be executed in a clock cycle in the above conventional CPU.

Therefore, as shown in Fig. 2, another conventional CPU 5 for accessing to a main memory 2 comprises:

a plurality of internal arithmetic circuitries 3; and

a cache memory 6 for exchanging data or instruction with the main memory 2 at the low access speed of the main memory 2 and exchanging the data or the instruction with the arithmetic circuitries 3 at the high speed of the arithmetic circuitry 3.

In the above configuration, a plurality of data or instructions are processed in parallel.

Accordingly, processing capacity can be improved more than the shortening of the clock cycle because the plurality of data or instructions can be processed in parallel.

However, in the above configuration, it occurs that the plurality of internal arithmetic circuitries 3 simultaneously access to the cache memory 6. In this case, if the cache memory 6 is provided with only one input/output port for the plurality of internal arithmetic circuitries 3, only one internal arithmetic circuitry 3 can access to the cache memory 6, while the other arithmetic circuitries 3 can not access to the cache memory 6.

Therefore, arithmetic processing in most of the arithmetic circuitries 3, which can not access to the cache memory 6, is stopped and processing capacity is declined. Also, the configuration for determining the order receiving the memory access requirement provided from each arithmetic circuitry 3 is complicated.

Therefore, if the cache memory 6 is changed to a multiport cache memory and each arithmetic circuitry 3 can independently access to the cache memory 6, the drawback in the conventional CPU 5 is solved and the advantage of the plurality of arithmetic circuitries 3 is demonstrated.

However, in the case that the multiport cache memory is utilized according to the plurality of arithmetic circuitries 3, either a load instruction or a store instruction according to the arithmetic processing in the arithmetic circuitry 3 is provided to each port of the multiport cache memory. Therefore, in the ports of the multiport cache memory, both the load and store instructions must be processed respectively. That is, each port of the multiport cache memory comprises a read/write port in which read operation and write operation are capable.

Accordingly, when all of the ports in the multiport cache memory is changed to the read/write ports, the number of wires connected to a memory cell 7 increases so that the area occupied by each ports of the multiport cache memory increases as shown in Fig. 3.

Moreover, as shown in Fig. 3, data input/output operation between the memory cell 7 and the external circuitry is executed through a pair of bit lines. Therefore, the number of bit lines in pairs increases so that mutual interference between bit lines easily occurs. As a result, the circuit design is complicated to prevent that the access operation is unstable.

SUMMARY OF THE INVENTION

It is one object of the present invention to provide a multiport cache memory in which the access operations of a plurality of arithmetic circuitries are simultaneously executed and the reduction of the configuration and the improvement of the reliability are achieved.

The object is achieved by the provision of a multiport cache memory for exchanging data or instructions with a plurality of arithmetic circuitries independently according to a load instruction or a store instruction provided from a CPU, comprising:

a plurality of read only ports (PR) for respectively transmitting the data or the instructions to each arithmetic circuitry according to the load instruction; and

a plurality of read/write ports (PW) for respectively transmitting the data or the instructions from/to each arithmetic circuitry according to the load or store instruction.

In the above configuration, the read only ports relate to only the load instruction, while the read/write ports relate to both the load and store instructions. Therefore, when the load instruction is provided from the CPU to the multiport cache memory, the data or the instruction is transmitted from the multiport cache memory to the arithmetic circuitry through the read only port. On the other hand, when the store instruction is provided from the CPU to the multiport cache memory, the data or the instruction is transmitted from the arithmetic circuitry to the multiport cache memory through the read/write port.

Accordingly, the structure of the ports in the multiport cache memory can be reduced because the read only port is more simple than the read/write port.

It is preferable that the number of read only ports (PR) be more than the number of read/write ports (PW) according to the statistical ratio of load instruction to the store instruction.

In the above configuration, the number of read only ports is determined according to the statistical ratio of load instruction to the store instruction. Therefore, the size of the multiport cache memory according to the present invention is optimized to reduce the occupied area.

Accordingly, the multiport cache memory can efficiently be operated according to the load and store instructions provided from the CPU.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a conventional CPU being provided with a cache memory and an arithmetic circuitry.

Fig. 2 is a block diagram of another conventional CPU being provided with a cache memory and a plurality of arithmetic circuitries.

Fig. 3 is a schematic circuit of the port in the cache memory shown in Figs. 1 and 2.

Fig. 4 is a schematic view of a multiport cache memory according to the present invention for showing the operation in the memory.

Fig. 5 is a schematic circuit of the ports in the multiport cache memory shown in Fig. 4.

DESCRIPTION OF THE SPECIFIC EMBODIMENT

Preferred embodiment of a multiport cache memory according to the present invention is described with reference to Figs. 4, 5.

Fig. 4 is a schematic view of a multiport cache memory according to the present invention for showing the operation in the memory.

As shown in Fig. 4, the multiport cache memory 11 for exchanging data or instructions with a plurality of arithmetic circuitries (not shown) independently according to a load instruction or a store instruction provided from the CPU (not shown), comprises:

read only ports PR for respectively transmitting the data or the instructions to each arithmetic circuitry according to the load instruction, the ports PR being m (m<n) in number; and

read/write ports PW for respectively transmitting the data or the instructions from/to each arithmetic circuitry according to the load or store instruction, the ports PW being n-m in number.

In the above configuration, the read only port PR is provided relate to the load instruction provided from the CPU so that the data or the instruction is transmitted from the multiport cache memory 11 to the corresponding arithmetic circuitry under the control of the load instruction. On the other hand, the read/write port PW is provided relate to the load and store instructions provided from the CPU so that the data or the instruction is transmitted in the same manner as in the read only port PR when the CPU provides the load instruction to the cache memory, while the data or the instruction is transmitted to the multiport cache memory 11 from the corresponding arithmetic circuitry under the control of the store instruction.

In this embodiment, the number of read only ports PR is more than the number of read/write ports PW . That is, m> n-m. The reason is as follows.

The number of load instructions is one-sidedly more than the number of store instructions as a result of statistical comparison.

Accordingly, because all of the ports in the multiport cache memory comprises read/write ports PW (n-m in number)and read only ports PR (m in number) which are more than the read/write ports PW in number, a plurality of access required from the CPU can simultaneously be executed even if write port PW is reduced.

Next, the operation in the multiport cache memory 11 is described in detail with reference to Fig. 5.

Fig. 5 is a schematic circuit of the ports in the multiport cache memory shown in Fig. 4, showing the configuration of a memory cell relate to a bit and wires.

As shown in Fig. 5, the multiport cache memory 11 comprises:

a plurality of memory cells 12, one bit of the data or the instruction being stored in each memory cell 12;

input/output circuits 13 (n-m in number), each circuit 13 corresponding to the read/write port PW;

a plurality of paired bit lines BL, $\overline{BL}$ for respectively transmitting the data or the instruction between the memory cell 12 and the input/output circuit 13, the bit lines BL, $\overline{BL}$ being n-m pairs and each bit lines BL, $\overline{BL}$ being connected to every memory cells 12 in parallel;

a plurality of sense amplifiers (SA) 14 (m in number) for respectively amplifying the data signal or the instruction signal being read from the designated memory cell 12, each SA 14 corresponding to the read only port PR; and

a plurality of bit lines BL (m in number) for respectively transmitting the data or the instruction from the designated memory cell 12 to the corresponding read only ports PR through the corresponding SA 14, and each bit lines BL being connected to every memory cells 12 in parallel.

The memory cell 12 comprises:

a latch circuit 15 for storing one bit of the data or the instruction, the circuit 15 including two inverters which are respectively connected an input terminal of a inverter with an output terminal of another inverter;

a plurality of field effect transistors (FET) 16 (m in number) which turn on when one bit signal stored in the latch circuit 15 is provided to the gate thereof;

a plurality of FETs 17 for transmitting the one bit signal to a corresponding read only port PR through a corresponding bit line BL when the FET 17 receives a word signal from a corresponding word line WL to the gate thereof; and

a plurality of paired transfer gates 18, 19 (n-m pairs in number) for controlling one bit signal passing between the latch circuit 15 and a corresponding paired bit lines BL, $\overline{BL}$, the gates 18, 19 turning on when a word signal provided from a corresponding word line WL is provided to the gates thereof.

In the above configuration, when an access requirement is provided from the CPU to a certain read only port PR, one bit signal stored in a specific latch circuit 15 which is designated by the CPU is read out to the read only port PR through a FET 16, a FET 17, a bit line BL, and an SA 14. In this case, the FET 17 is turned on by the corresponding word signal which is provided to the word line under the control of the CPU.

When an access requirement is provided from the CPU to a certain read/write port PW to read out one bit paired signals stored in a specific latch circuit 15 which is designated by the CPU, the signals are read out in parallel to the read/write port PW through a pair of transfer gates 18, 19, a pair of bit lines BL, $\overline{BL}$, an input/output circuit 13. In this case, the paired transfer gates 18, 19 are turned on by the corresponding word signals which are provided to the word lines under the control of the CPU.

When an access requirement is provided from the CPU to a certain read/write port PW to store one bit signal to a certain latch circuit 15, the signal is transmitted to the latch circuit 15 through an input/output circuit 13, a pair of bit lines BL, $\overline{BL}$, and a pair of transfer gates 18, 19. In this case, the paired transfer gates 18, 19 are turned on by the corresponding word signals which are provided to the word lines under the control of the CPU.

Therefore, as shown in Fig. 5, the number of paired bit lines BL, $\overline{BL}$ is two times as compared with the number of bit lines BL. Also, to read or write one bit signal through the read/write port PW, the input/output circuits 13 are necessary. The increase of the structure is more remarkable as the memory capacity is increased. In other word, if all of the ports are read/write ports PW, the multiport cache memory is too large to process the data or the instruction.

Accordingly, because most of the ports are read only ports in this embodiment, the occupied area can dramatically be reduced in the integrated circuit as compared with the conventional multiport cache memory in which all of the ports are read/write ports PW.

Also, in the read only port PR, one bit data read from the latch circuit 15 is provided to the gate of the FET 16, then the electric potential of the bit line connected to the SA 14 is changed according to the condition of the FET 16 which is turned on or off under the control of the CPU. The electric potential transmitted to the SA 14 is amplified so that one bit data is read out. Therefore, the stored data is not affected by the other data stored in the other latch circuit. In other words, the reading operation is stably executed.

On the other hand, when one bit data stored in the latch circuit 15 is read out to the outside through the read/write port PW, the data is read out to the paired bit lines BL, $\overline{BL}$ through the transfer gates 18, 19. Therefore, the data of the other latch circuit or the surrounding noises are stored to the latch circuit 14 through the paired bit lines BL, $\overline{BL}$ so that the proper data is deleted.

Therefore, to prevent the above influence in the conventional multiport cache memory, the circuitry including the latch circuit 15 in the memory cell 12, the transfer gates 18, 19, the loaded transistors of the bit lines, and the like must be optimized to stabilize the reading operation.

However, in the present invention, because the number of the read only ports PR is more than the number of the read/write ports PW, the stability of the reading operation can be improved and the complication of the circuit design can be avoided.

Having illustrated and described the principles of our invention in a preferred embodiment thereof,

it should be readily apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications coming within the spirit and scope of the accompanying claims.

Claims

1. A multiport cache memory for exchanging data or instructions with a plurality of arithmetic circuitries independently according to a load instruction or a store instruction provided from a CPU, comprising:

   a plurality of read only ports (PR) for respectively transmitting the data or the instructions to each arithmetic circuitry according to the load instruction; and

   a plurality of read/write ports (PW) for respectively transmitting the data or the instructions from/to each arithmetic circuitry according to the load or store instruction.

2. A multiport cache memory according to claim 1 in which the number of read only ports (PR) is more than the number of read/write ports (PW) according to the statistical ratio of load instruction to the store instruction.

FIG.1

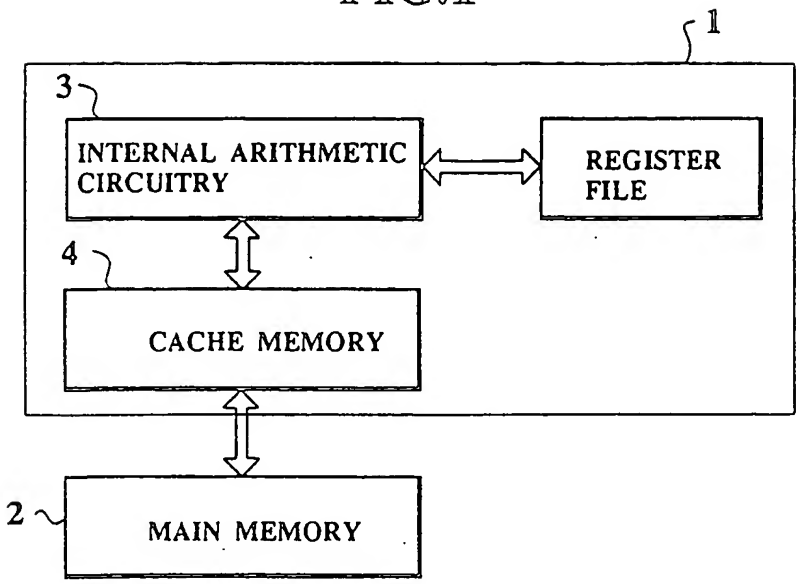

1
3
INTERNAL ARITHMETIC CIRCUITRY
REGISTER FILE
4
CACHE MEMORY
2
MAIN MEMORY

FIG.2

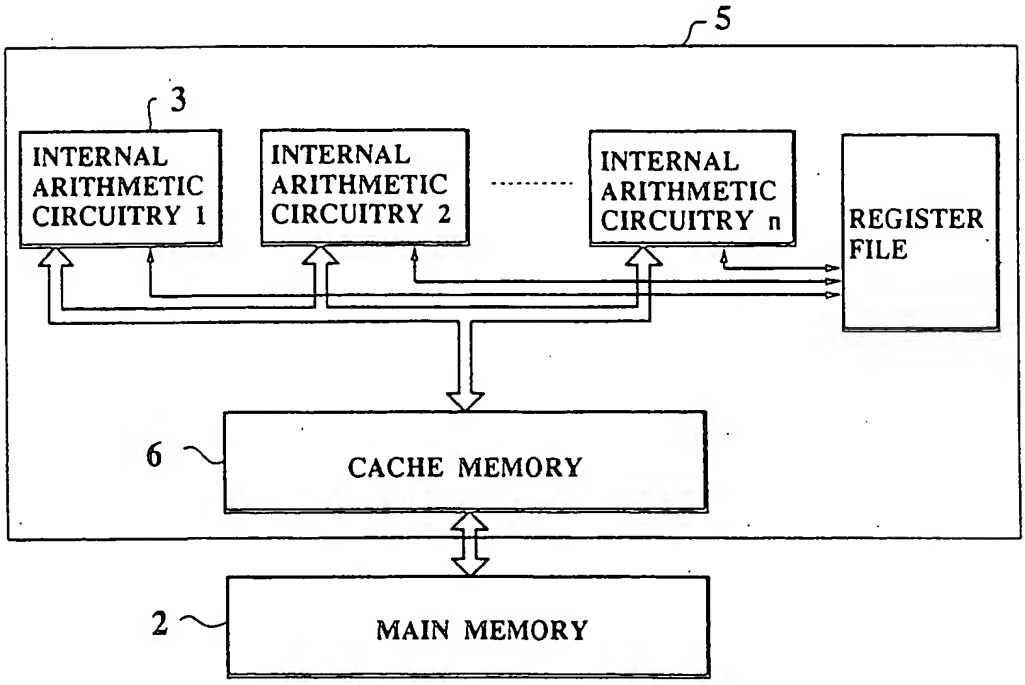

5
3
INTERNAL ARITHMETIC CIRCUITRY 1
INTERNAL ARITHMETIC CIRCUITRY 2
INTERNAL ARITHMETIC CIRCUITRY n
REGISTER FILE
6
CACHE MEMORY
2
MAIN MEMORY

FIG.3

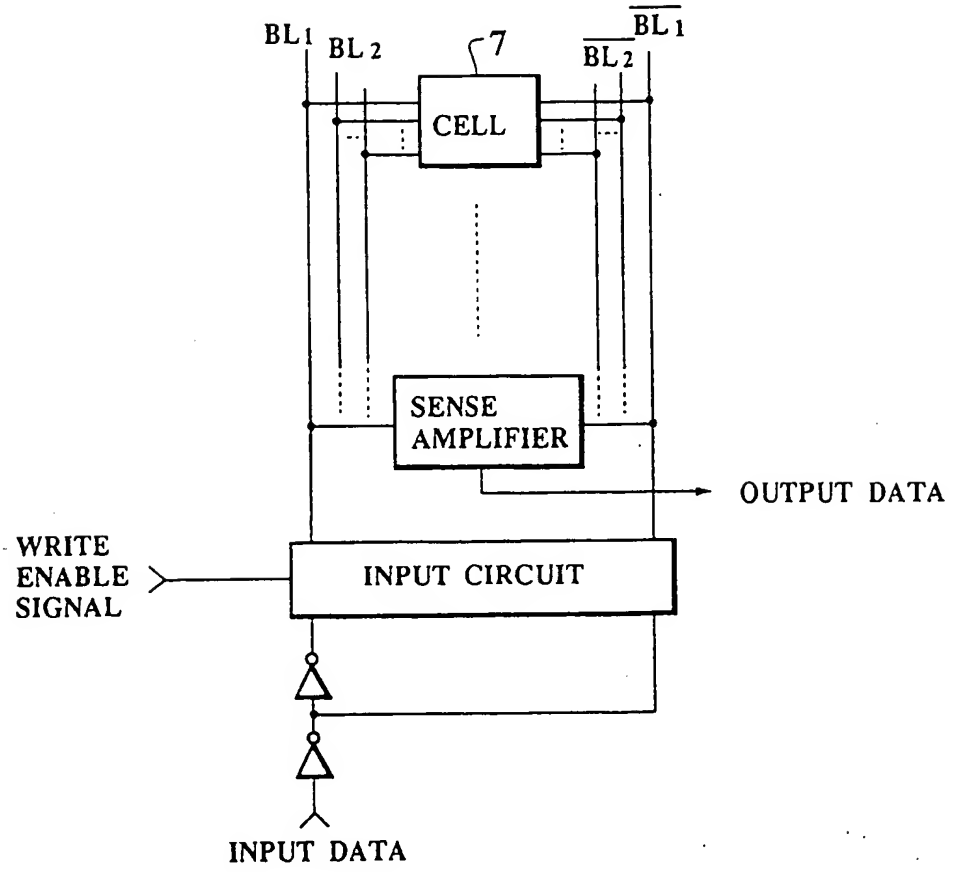

BL1
BL2
7
$\overline{BL_2}$
$\overline{BL_1}$
CELL
SENSE AMPLIFIER
OUTPUT DATA
WRITE ENABLE SIGNAL
INPUT CIRCUIT
INPUT DATA

FIG.4

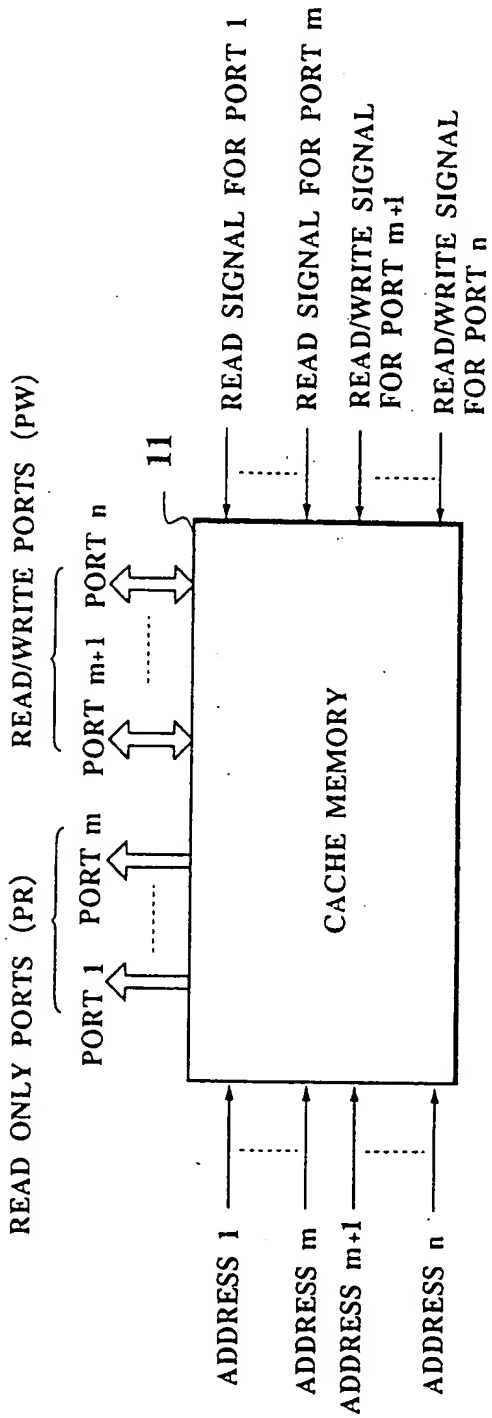
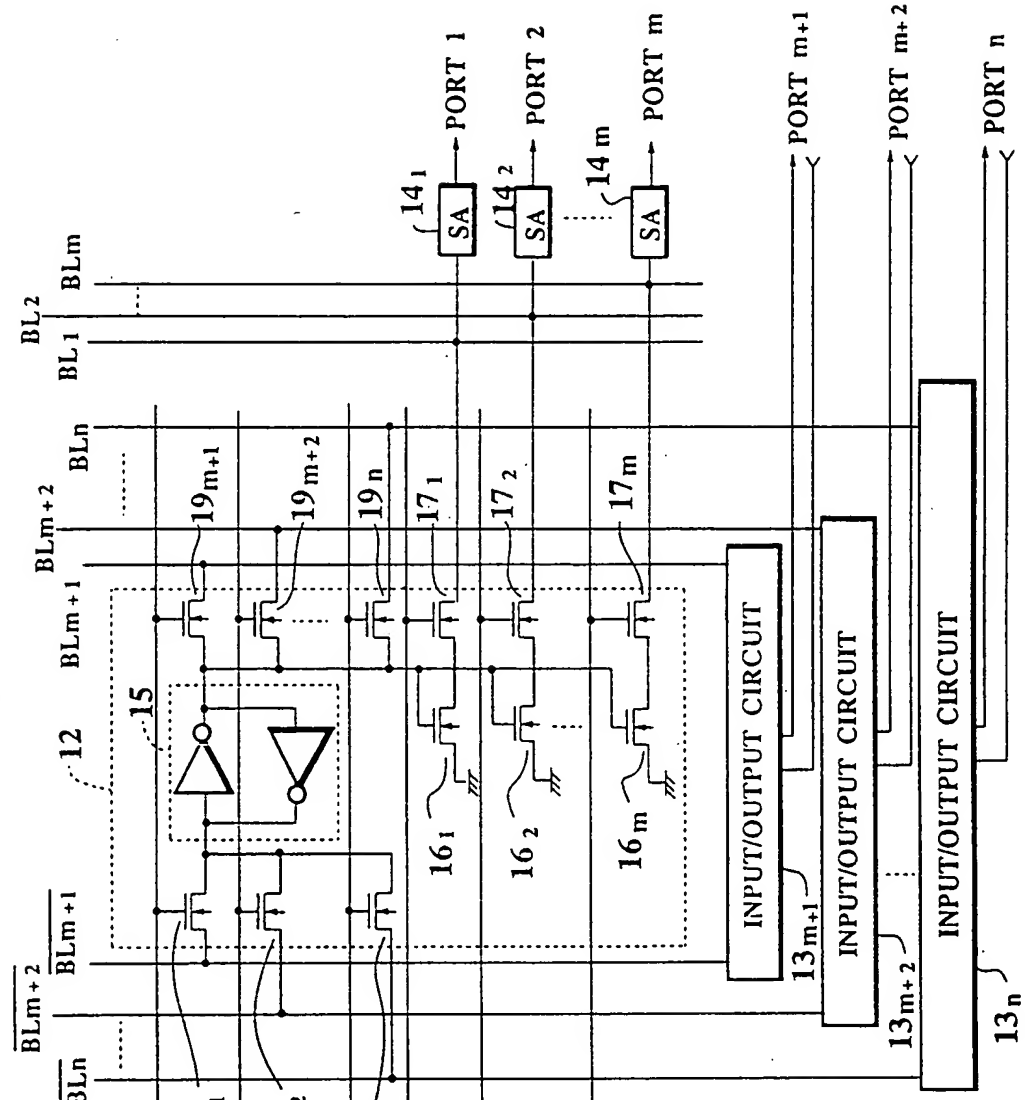

READ ONLY PORTS (PR)
READ/WRITE PORTS (PW)
PORT 1
PORT m
PORT m+1
PORT n
11
CACHE MEMORY
READ SIGNAL FOR PORT 1
READ SIGNAL FOR PORT m
READ/WRITE SIGNAL FOR PORT m+1
READ/WRITE SIGNAL FOR PORT n
ADDRESS 1
ADDRESS m
ADDRESS m+1
ADDRESS n

FIG.5


WLm+1
WLm+2
WLn
WL1
WL2
WLm
18m+1
18m+2
18n
BLn
BLm+2
BLm+1
BLm
BL2
BL1
12
15
19m+1
19m+2
19n
17 1
17 2
17m
16 1
16 2
16m
14 1
14 2
14 m
SA
PORT 1
PORT 2
PORT m
PORT m+1
PORT m+2
PORT n
INPUT/OUTPUT CIRCUIT
13m+1
13m+2
13n

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(54) **Multiport cache memory.**

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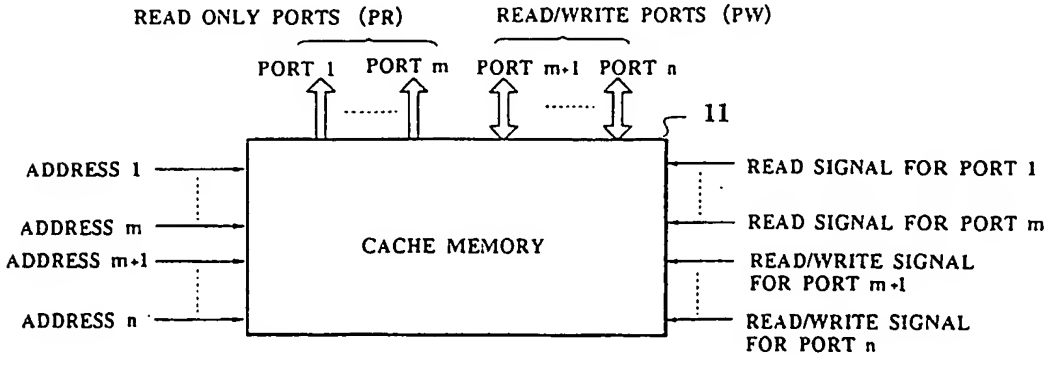
FIG.4



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EUROPEAN SEARCH REPORT

Application Number

EP 91 11 2338

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-0 376 253 (TOSHIBA) * column 4, line 32 - column 5, line 21; figures 3,5 *	1,2	G06F12/08
Y	EP-A-0 297 571 (NATIONAL SEMICONDUCTOR CORP.) * abstract; figure 4 *	1,2	
A	EP-A-0 340 668 (HITACHI) * abstract; figures 1,2,4 *	1,2	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G06F G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 SEPTEMBER 1992	NIELSEN O.P.

CATEGORY OF CITED DOCUMENTS

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